

## 40G QSFP+ ER4 40km Optical Transceiver GQS-SPO400-ER4C

### Features

- ✓ Hot-pluggable QSFP form factor
- ✓ Supports 39.8 Gb/s to 44.6 Gb/s
- ✓ 18.5 dB link insertion loss budget
- ✓ Single 3.3V power supply
- ✓ Maximum link length of 40km on Single Mode Fiber (SMF)
- ✓ Uncooled 4x10Gb/s CWDM transmitter
- ✓ XLPPI electrical interface
- ✓ Duplex LC receptacles
- ✓ Operating case temperature range: 0 to 70°C
- ✓ 3.5W maximum power dissipation
- ✓ **RoHS-6 compliant (lead free)**



### Applications

- ✓ 40GBASE-ER4 40G Ethernet
- ✓ OTU3, OTU3e1, OTU3e2

### Description

Gigalight's 40GE QSFP+ ER4 40km Optical Transceiver modules are designed for using in 40 Gigabit Ethernet and 4X10G OTN client interfaces over single mode fiber. They are compliant with the QSFP+ MSA, IEEE 802.3bm 40GBASE-ER4, and OTU3 requirements. The Gigalight technology enables the integration of 4 transmitters, 4 receivers and an optical MUX/DeMUX into a small form factor package

### Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>cc</sub>	-0.3	3.6	V

Input Voltage	$V_{in}$	-0.3	$V_{cc}+0.3$	V
Storage Temperature	$T_s$	-20	85	°C
Case Operating Temperature	$T_c$	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

## Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	$V_{cc}$	3.13	3.3	3.47	V
Operating Case Temperature	$T_c$	0		70	°C
Data Rate Per Lane	fd	9.95	10.3125	11.15	Gb/s
Humidity	Rh	10		90	%
Power Dissipation	$P_m$			3.5	W
Fiber Bend Radius	$R_b$	3			cm

## Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	$Z_{in}$	90	100	110	ohm
Differential Output Impedance	$Z_{out}$	90	100	110	ohm
Differential Input Voltage Amplitude <sup>1</sup>	$\Delta V_{in}$	300		1100	mVp-p
Differential Output Voltage Amplitude <sup>2</sup>	$\Delta V_{out}$	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER		E-12		
Input Logic Level High	$V_{IH}$	2.0		$V_{cc}$	V
Input Logic Level Low	$V_{IL}$	0		0.8	V
Output Logic Level High	$V_{OH}$	$V_{cc}-0.5$		$V_{cc}$	V
Output Logic Level Low	$V_{OL}$	0		0.4	V

### Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
<b>Transmitter</b>					
Signaling Speed per Lane		9.95	10.3	11.15	GBd
Center Wavelength	$\lambda_c$	1264.5	1271	1277.5	nm
		1284.5	1291	1297.5	

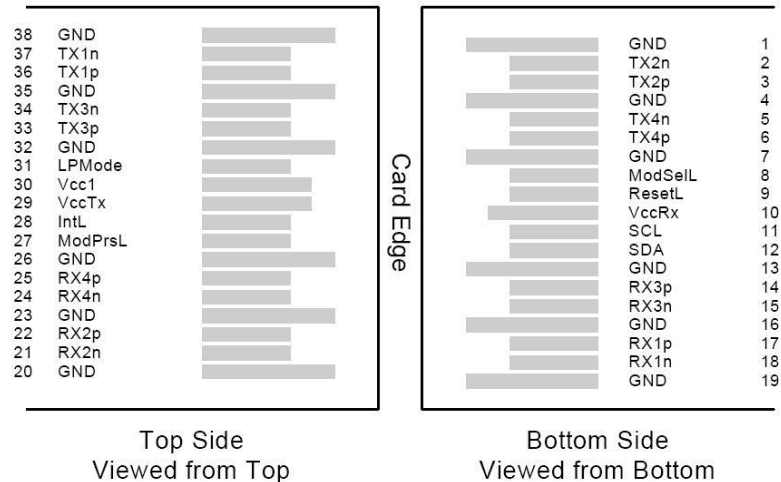
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Total Average Launch Power	$P_{out}$			10.5	dBm
Transmit OMA per Lane		-1.3		5	dBm
Average Optical power per lane	TXPX	-2.7		4.5	dBm
Difference in launch power between any two lanes (OMA)				4.7	dB
Transmitter Dispersion Penalty	TDP			2.6	dB
Launch power (OMA) minus TDP per lane		-0.5			dBm
Extinction Ratio	ER	4.5			dB
Sidemode Suppression ratio	SSRmin	30			dB
Average Launch Power of OFF Transmitter (each lane)	$P_{off}$			-30	dB
Relative Intensity Noise	RIN			-128	dB/Hz
Transmitter Eye Mask definition: X1, X2, X3, Y1, Y2, Y3		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Jitter Generation		Per OTL3.4 section 4.14.1			
<b>Receiver</b>					
Signaling Speed per Lane		9.95		11.15	GBd
Center Wavelength	$\lambda_c$	1264.5	1271	1277.5	nm
		1284.5	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Receive Power (OMA) per Lane	RxOMA			-4.0	dBm
Average Receive Power per Lane	RXPx	-21.2		-4.5	dBm
Receiver Sensitivity (OMA) per Lane(@ PRBS $2^{31-1}$ and BER= $5 \times E^{-5}$ )	Rxsens			-19	dBm
Stressed Receiver Sensitivity (OMA)per Lane(@ PRBS $2^{31-1}$ and BER= $10^{-12}$ )	SRS			-16.8	dBm
Damage Threshold per Lane	PMAX			3.8	dBm
Return Loss	RL			-26	dB
Jitter Tolerance		Per OTL3.4, G.8251			
Vertical eye closure penalty, per lane				2.2	dB
Receive electrical 3 dB upper cutoff frequency, per lane				12.3	GHz
LOS Assert	LOS <sub>A</sub>	-35			dBm
LOS De-Assert – OMA	LOS <sub>D</sub>			-19	dBm
LOS Hysteresis	LOS <sub>H</sub>	0.5			dB

## Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground <sup>1</sup>
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground <sup>1</sup>
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground <sup>1</sup>
8	LVTTL-I	MODSEIL	Module Select <sup>2</sup>
9	LVTTL-I	ResetL	Module Reset <sup>2</sup>
10		VCCRx	+3.3V Receiver Power Supply
11	LVC MOS-I	SCL	2-wire Serial interface clock <sup>2</sup>
12	LVC MOS-I/O	SDA	2-wire Serial interface data <sup>2</sup>
13		GND	Module Ground <sup>1</sup>
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground <sup>1</sup>
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground <sup>1</sup>
20		GND	Module Ground <sup>1</sup>
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground <sup>1</sup>
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground <sup>1</sup>
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board <sup>2</sup>
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMODE	Low Power Mode <sup>2</sup>
32		GND	Module Ground <sup>1</sup>
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground <sup>1</sup>
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground <sup>1</sup>

**Note:**

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.



**Figure 1. Electrical Pin-out Details**

### ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

### ResetL Pin

Reset. LPMode\_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time ( $t_{init}$ ) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset ( $t_{init}$ ) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

### LPMode Pin

Gigalight QSFP+ modules operate in the low power mode (less than 3.5 W power consumption). This pin active high will decrease power consumption to less than 3W.

### ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

### IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

## Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on <sup>1</sup> , hot plug or rising edge of Reset until the module is fully functional <sup>2</sup>
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on <sup>1</sup> until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on <sup>1</sup> to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional <sup>2</sup>
LPMMode Assert Time	ton_LPMMode	100	μs	Time from assertion of LPMMode ( $V_{in}$ : LPMMode= $V_{IH}$ ) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until $V_{out}$ : IntL= $V_{OL}$
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read <sup>3</sup> operation of associated flag until $V_{out}$ : IntL= $V_{OH}$ . This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set <sup>4</sup> until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared <sup>4</sup> until associated IntL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set <sup>4</sup> until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared <sup>4</sup> until the module is fully functional <sup>3</sup>

**Note:**

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.

4. Measured from falling clock edge after stop bit of write transaction.

## Mechanical Dimensions

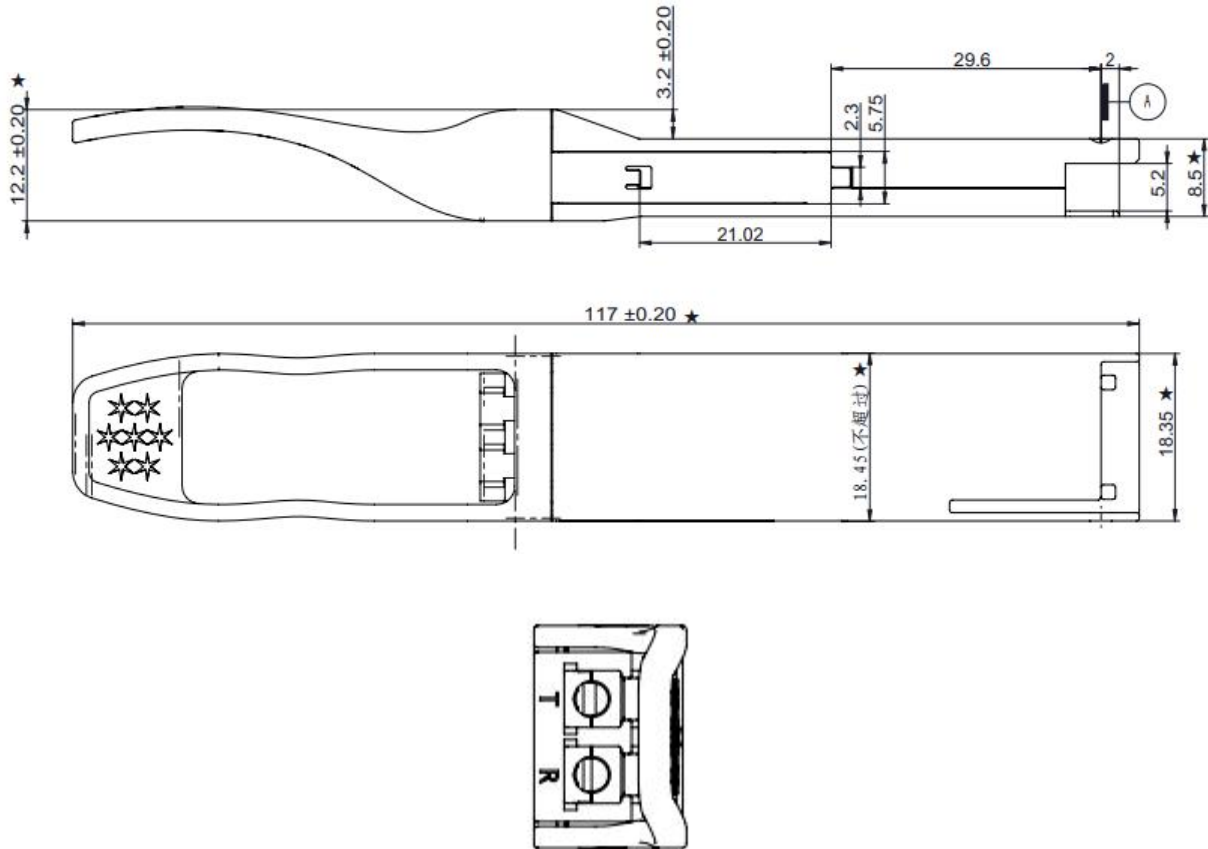


Figure 2. Mechanical Specifications

## Regulatory Compliance

Gigalight's QQS-SPO400-ER4C QSFP transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Laser Eye Safety	TÜV	EN 60825-1:2007 EN 60825-2:2004+A1+A2
Electrical Safety	TÜV	EN 60950
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

## References

1. QSFP+ MSA
2. Ethernet 40GBASE-ER4 IEEE802.3bm
3. ITU-T G.695: Optical Interfaces for Coarse Wavelength Division Multiplexing Applications, October 2010.
4. Directive 2011/65/EU of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment”. Certain products may use one or more exemptions as allowed by the Directive.

### CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Ordering Information

Part Number	Product Description
GQS-SPO400-ER4C	40GE/OTU3 QSFP ER4, 40km on single-mode fiber

## Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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## Revision History

Revision	Date	Description
V0	Jun-5-2019	Advance Release.